Finite Element Modeling Predicts the Effects of Voids on Thermal Shock Reliability and Thermal Resistance of Power Device

The thermal-mechanical effects of void size and location in lead-free solder heat-sink attachment of power devices is investigated

BY J. CHANG, L. WANG, J. DIRK, AND X. XIE

ABSTRACT. Three-dimensional finite element modeling (FEM) analysis was conducted to investigate the effects of the void size and location on the reliability of Sn-Ag-Cu heat-sink attachment. The results showed that void size does not have a significant effect on the strain/stress distribution, unless it is near the corner of the solder attachment, a location originally with higher stress. This is generally in agreement with the experimental results that a heat-sink attachment with an average of 37.5% void can survive more than 3000 cycles of thermal shock at –40° to 125°C. The void size had a significant effect on thermal dissipation. A 20% voids would cause the chip temperature to rise more than 5.1°C, which would obviously degrade the reliability of the device. Compared to void size, the location of voids is less significant. Void size of 10% at a different location causes chip temperature variation around 1°C.

Introduction

The reliability of the semiconductor devices is critical for designers and manufacturers. Electronic power devices are developed with increasing power capability, high voltage, and high current (Ref. 1). The typical loads for electronic power devices are high temperatures and temperature changes. As reported, in a typical power device, 4% of controlled power is dissipated as heat in the device. So thermal and thermal-mechanical management is important for power devices (Ref. 1).

In a power device assembly, materials with different thermal and mechanical properties are bonded together to constitute a complicated system. The cyclic stress/strain will be produced in the assembly due to the coefficient of thermal expansion (CTE) mismatch of different layers during operation (Ref. 2). Soft solder is often used for the heat-sink attachment because it has very good mechanical and heat dissipation performance; also, it allows plastic deformation, so that stresses due to temperature excursions and CTE mismatches during device service can be relaxed (Ref. 3). But accumulations of the plastic deformation may produce solder fatigue cracks and eventually cause the failure of the solder attachment.

Reliability of the most commonly used Sn-Pb eutectic solder has been extensively investigated and has been well understood. However, due to environmental and health concerns, Sn-Pb eutectic solder is being replaced by lead-free solders, among which Sn-Ag-Cu is the dominant candidate for use in reflow soldering technology (Ref. 4). Although quite a large number of studies have concentrated on this new alloy system from laboratory research to small-scale production, more data are needed before a solid understanding can be established.

Voids are easily formed in the solder joint. It became a more critical problem when lead-free solder was used in recent years because of its comparatively poor solderability. Voids are formed due to the outgassing of flux entrapped in the solder joint during reflow (Ref. 5). The solder paste contains 35~65 vol-% volatile materials. The outgassing is generally produced by the evaporation of solvent and additives in the solder paste. Some gases may be entrapped between the printed circuit board (PCB) and components causing voids to be formed during cooling. Previous studies have indicated that the reflow process and solder materials are the most significant factors that affect void formation (Refs. 6, 7).

There are no universal criteria regarding void size and location (Ref. 8). The factors that affect void formation are complex, and it is difficult to study the effect of void on reliability because many variables in the assembly process are not controllable regarding void formation. Most studies about the effect of voids on reliability are focused on Sn-Pb eutectic solder in BGA/CSP joints (Refs. 8, 9). The results show that big voids, especially when the voids are greater than 50% of the solder joint area, had been considered one of the critical issues in joint strength and reliability. Small voids also have effects on reliability, but it is dependent on the number and location.

From the thermal point of view, voids in solder layers become one of the main defects affecting the heat dissipation (Ref. 10). The overall effect of voids is to decrease the solder cross-section area available for heat dissipation. The heat dissipation is especially important for power devices. Industrial practices often set 10% voids as the highest limit for general heat-sink attachment and 5% for higher requirements.

This paper investigates the effect of void size and location in Sn-Ag-Cu heat-sink attachment on the thermal shock reliability and thermal resistance of power devices using 3-D finite element modeling (FEM). The degradation of heat-sink attachment by SnAgCu lead-free solder during thermal shock has been verified by experiment. Samples with high voiding percentages were selected for the investi-

KEYWORDS

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Equivalent Stress
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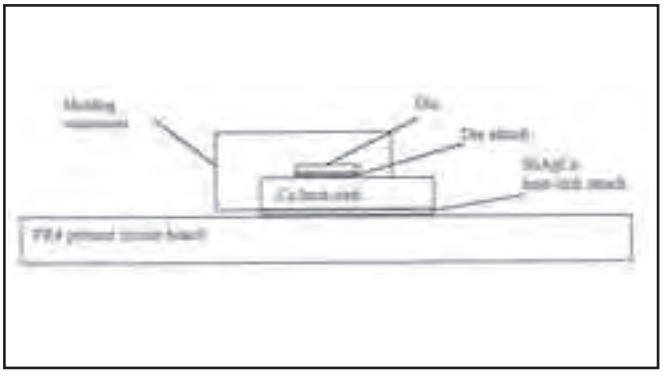


Fig. 1 — Schematic layout of structure.

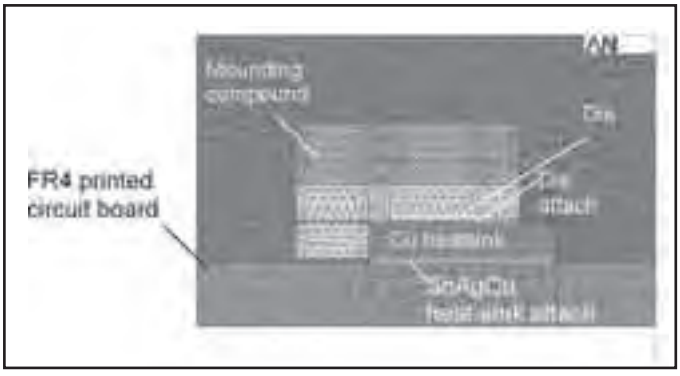


Fig. 2 — Simulation mesh model.

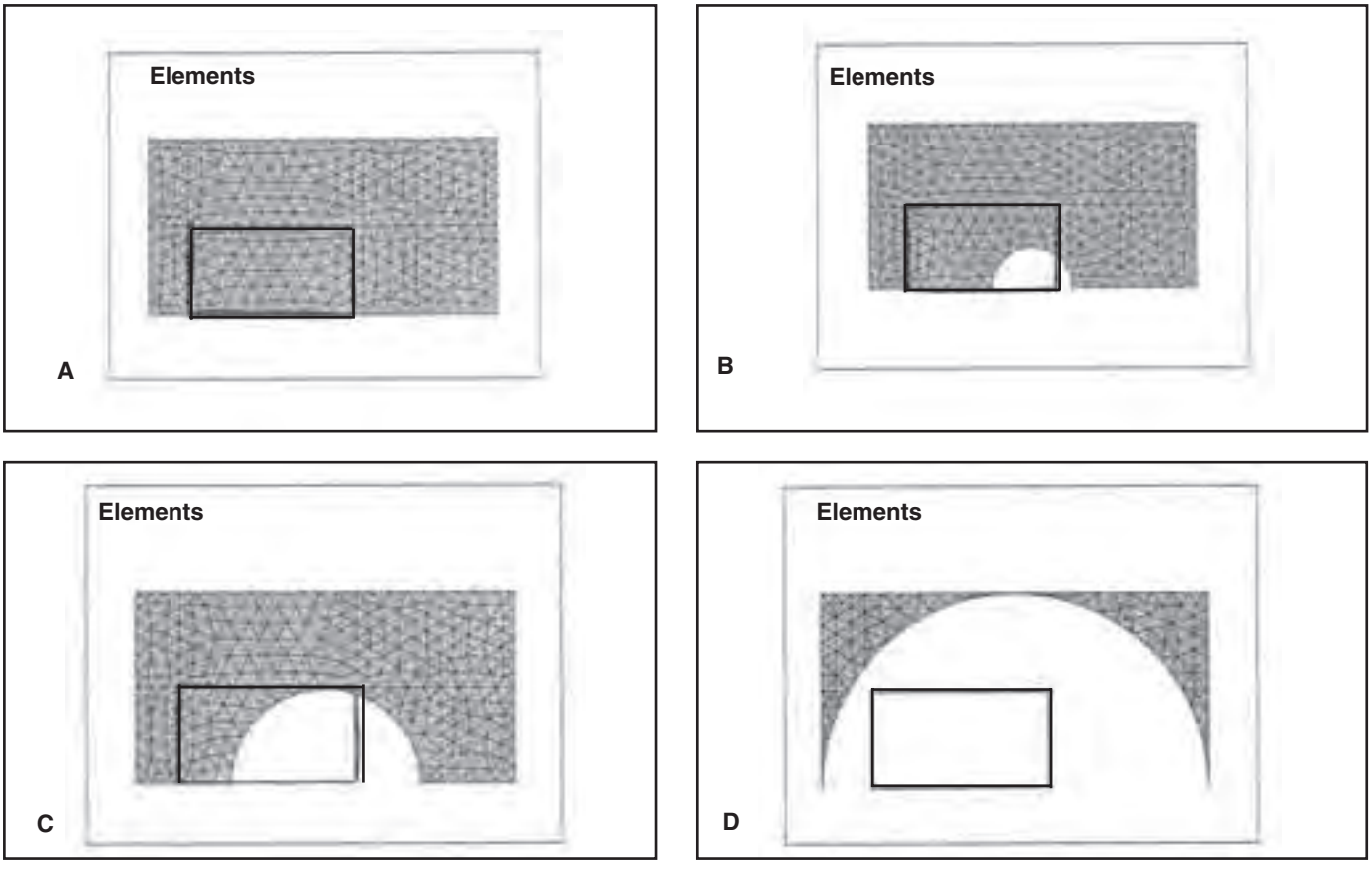


Fig. 3 — Heat-sink attachment model of different voiding percentages. (Black rectangle is the location of die.) A — 0%; B — 5%; C — 20%; and D — 79%.

Table 1 — Material Properties Used in the Simulation

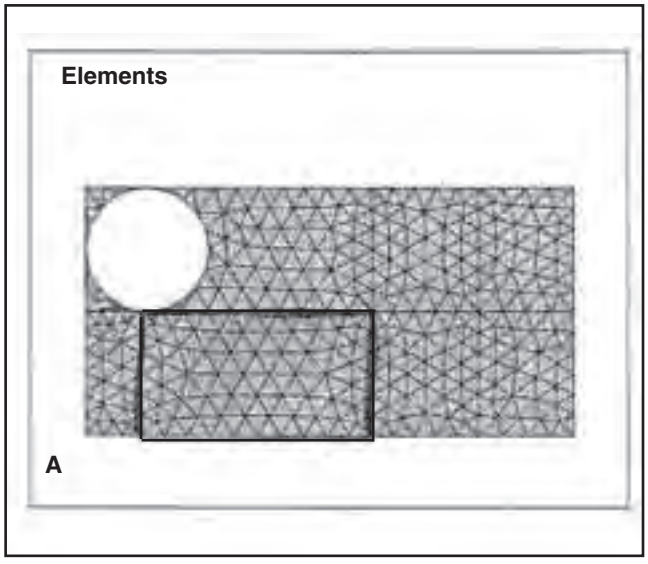
	Young's modulus (GPa)	CTE (ppm/°C)	Density, ρ ($x10^{-6}$kg/mm^3)	Specific heat, C_p (J/kg·°C)	Conductivity, K (W/mm·°C)	Poisson's ratio
Silicon	131	2.7	2.32	750	0.084	0.3
FR4	16	16	1.80	1260	2.0E-4	0.28
Copper	120	17	8.96	385	0.386	0.35
Sn3.0Ag0.5Cu	38.70-0.176 x T	25	8.41	192	0.050	0.35
Pb97.5Sn	24.1-0.028 x T	28	10.90	136	0.036	0.3
Molding	15	18	1.80	126	1.6E-3	0.3

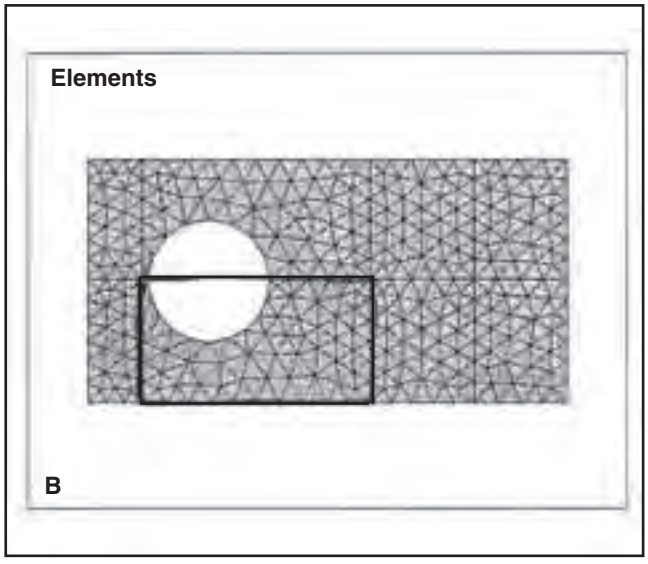
gation in order to get information on the significance of void formation on the reliability of SnAgCu heat-sink attachment. All FEM simulations were performed using *ANSYS* software.

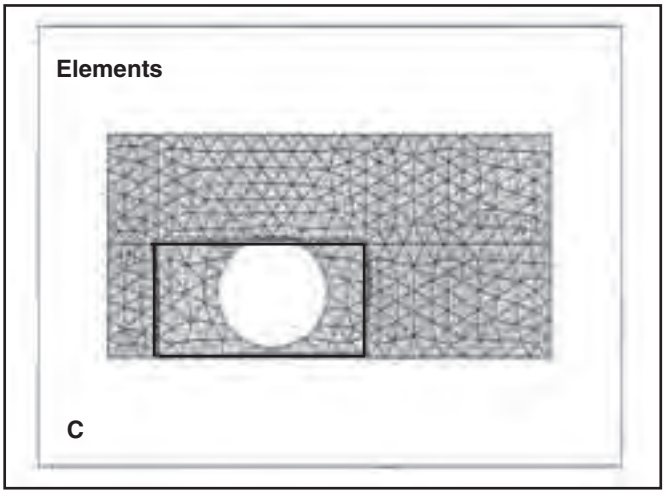
FEM Simulation on Thermal Mechanical Strain/Stress

Geometry Model and Material Properties

A DPAK device soldered on the PCB was selected for the simulation. The cross section of the geometry model is illustrated in Fig. 1. The device and substrate were bonded together with Sn3.0Ag0.5Cu







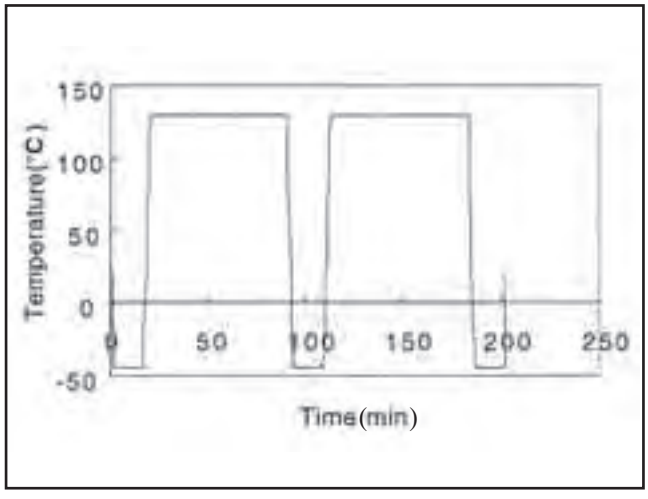


Fig. 4 — Heat-sink attachment model with voiding percentage of 10% at different locations. (Black rectangle is the location of die.) A — 10%-II; B — 10%-II; and C — 10%-III.

Fig. 5 — Cycles of temperature loading of simulation.

heat-sink attachment. Inside the package, a high lead solder Pb97Sn3 was used for die attachment. Since Sn3.0Ag0.5Cu solder and die attach Pb97Sn3 solder are viscoplastic in nature, the viscoplastic Anand model was used to present the Sn3.0Ag0.5Cu solder and die attach Pb97.5Sn solder behavior. All the other materials are considered to be elastic. Material properties used in this simulation are shown in Table 1 (Ref. 11). For Sn3.0Ag0.5Cu and Pb97Sn3 solder, material properties used in the Anand model are shown in Table 2 (Ref. 11).

Meshing Model and Loading Condition

Meshing Model

In this study, 3D-1/2th symmetric models were used. All voids in the heat-sink attachment were assumed to be circular and leads in the package were ignored for simplification. The mesh model is shown in Fig. 2. The geometry data were directly taken from a cross section of real specimen measurements.

The heat-sink attachment model with different void sizes and locations is shown in Figs. 3 and 4, respectively. The voiding percentages 5, 10, and 20% were selected as levels of interests, and a 79% void selected as a worst case reference. For 10% voids, three typical locations were chosen for the modeling and simulation.

Loading Conditions

Room temperature was taken as the zero stress point. It is assumed that viscoplastic deformations take place at all nonzero stress values. Figure 5 shows the cycles of temperature loading of the simulation. The start of thermal loading was at the stress-free state of 25°C. The dwell time at –40° and 125°C was 15 and 75 min, respectively. The ramp rate was 50°C/min.

Table 2 — Parameters Used in Anand Model

Material parameters	Sn3.0Ag0.5Cu	Pb97Sn3
A (sec^{-1})	5.87 x 10^6	3.25 x 10^4
Q/R (°K)	7460	15600
ξ	2.00	7.00
m	0.0942	0.0143
s (MPa)	58.3	72.7
n	0.015	0.00437
h_0 (MPa)	9350	1790
a	1.50	3.73
s_0 (MPa)	45.9	15.1

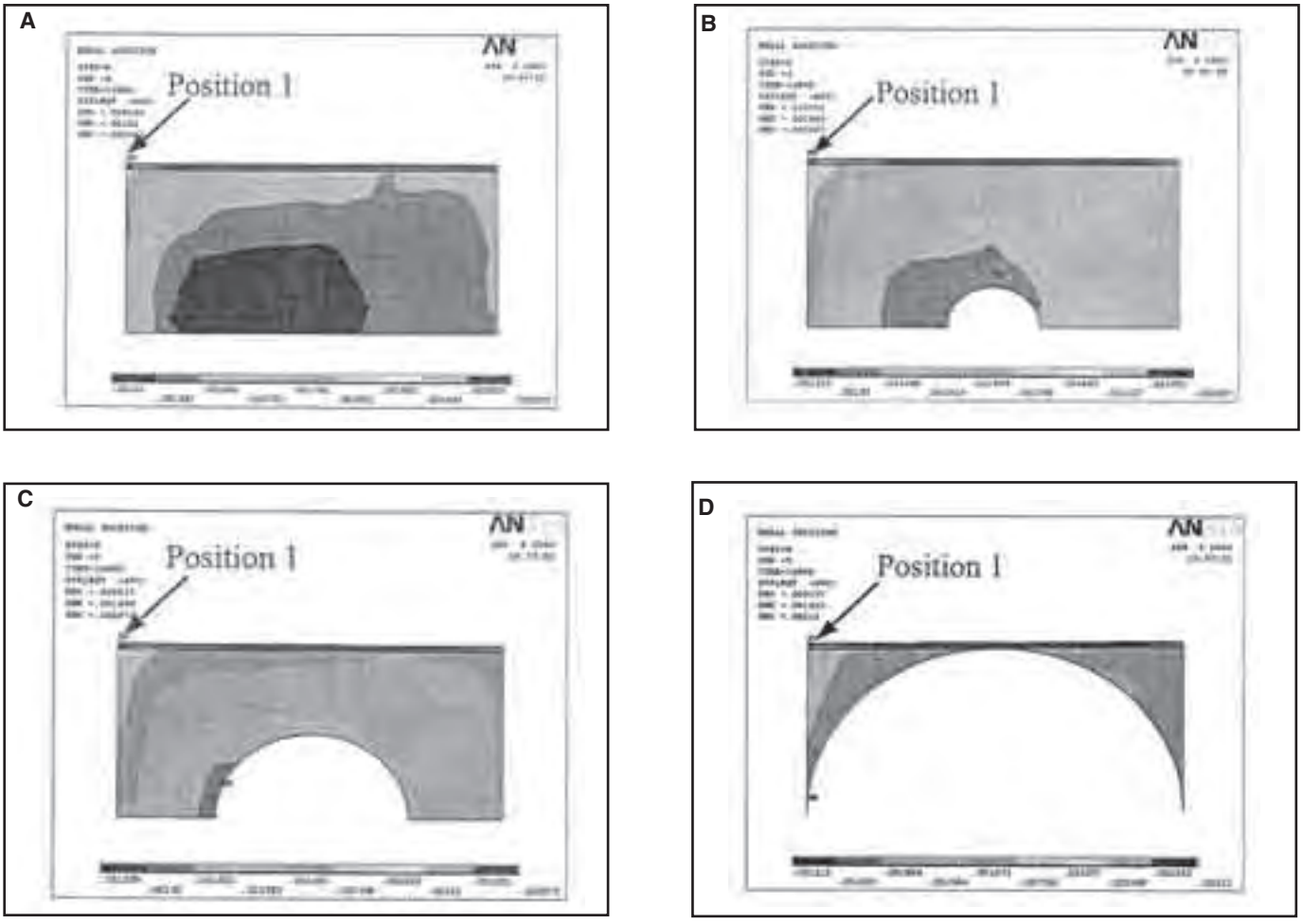


Fig . 6 — Equivalent plastic strain distribution in SnAgCu heat-sink attachment with different voiding percentages after 125°C dwell. A — 0%; B — 5%; C — 20%; and D — 79%.

Table 3 — Thermal Mechanical Simulation Results

Void percentages (%)	Maximum equivalent plastic strain (%)	Maximum equivalent stress	Increase in maximum equivalent plastic strain compared to no void (%)	Increase in maximum equivalent stress compared to no void (%)
0	0.2063	32.041	0	0
5	0.2067	32.055	0.194	0.044
20	0.2073	32.014	0.482	–0.084
79	0.2130	31.760	3.146	–0.885
10–I	0.2283	32.124	9.636	0.258
10–II	0.2054	31.904	–0.438	–0.429
10–III	0.2072	32.016	0.434	–0.078

The time/temperature profile was obtained from real measurement data. The simulations were performed for several cycles (typically 2 or 3 cycles) until the stress/strain hysteresis loop stabilized.

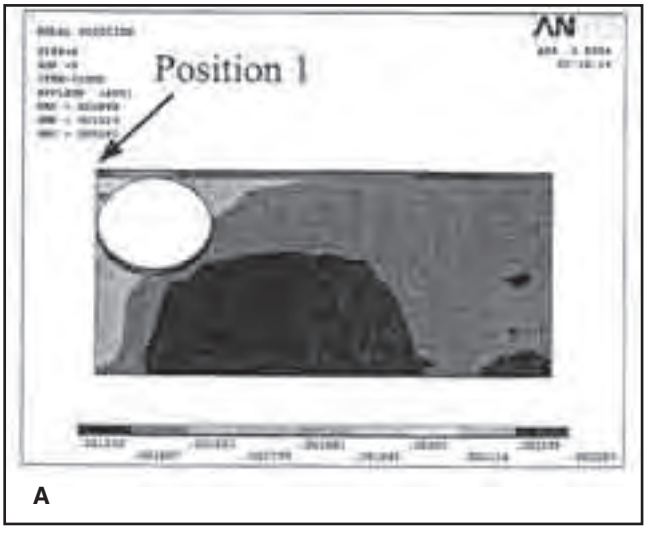
Thermal-Mechanical Strain/Stress Simulation Results

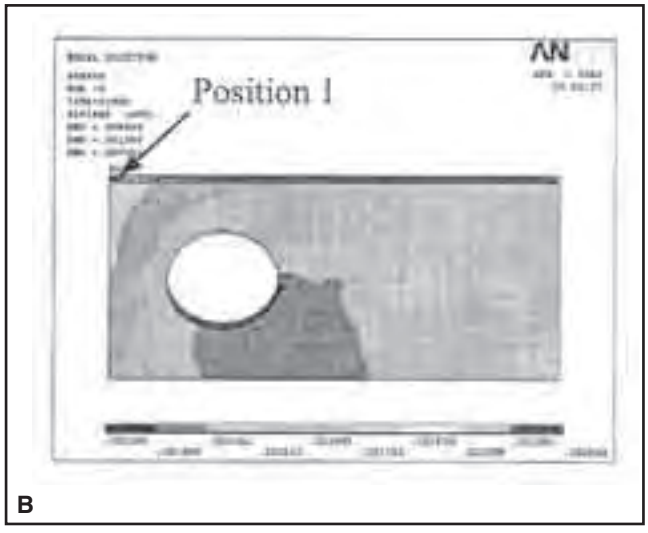
Equivalent plastic strain distribution of heat-sink attachment with different voiding percentages and different void locations after 125°C dwell are shown in Figs. 6 and 7, respectively. The maximum equivalent plastic strain occurred at the corner of the heat-sink attachment (position 1 in Figs. 6 and 7). Equivalent plastic strain distribution was circular. The outer heat-sink attachment had relatively larger equivalent plastic strain. The distribution of equivalent plastic strain distribution was almost the same for different voiding percentages and different void locations.

Maximum equivalent plastic strain and maximum equivalent stress of different void sizes and locations compared with the no void case is listed in Table 3. Void size had almost no effect on the maximum equivalent plastic strain. The increase in maximum equivalent plastic strain was less than 3.5%, even when the voiding percentages reached 79%, compared to the maximum equivalent plastic strain of no voids.

While void location affected the maximum equivalent plastic strain to some extent, the increase in maximum equivalent plastic strain reached 9.636% when the voids were at the corner of the heat-sink attachment (10%-I). The maximum equivalent plastic strain even decreased when the voids were at location 10%-I.

Maximum equivalent stress decreased in most cases except when the voiding percentages were 5 and 10%-I. But the changes in maximum equivalent stress were small ($< \pm 1\%$) whether for different void sizes or different void locations.





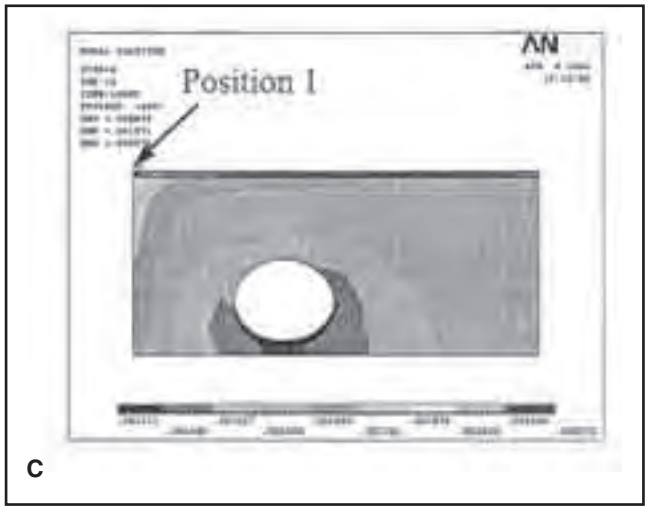


Fig. 7 — Equivalent plastic strain distribution of heat-sink attachment with different void location after 125°C dwell. A — 10%-I; B — 10%-II; and C — 10%-III.

Thermal Analysis

Thermal Analysis Loading Condition

For the thermal analysis, the simulation was based on a heat conduction equation. Chip was the only heat source in assembly. All the materials were assumed to be isotropic and uniform in thermal conductivity. The heat transfer coefficient at the topside of device was obtained through free convection just as vertical plate.

The exterior surface of the PCB board, except the region under the device, was set at 50°C. Chip power was 1 W and its volume was 2.4 x 2.58 x 0.22 mm^3, so its heat generation rate (heat flow per unit volume) was 0.73 W/mm^3.

Heat dissipation ability is characterized by thermal resistance with the following formula (Ref. 12):

$$R = \frac{\Delta T}{q} \qquad (1)$$

where ΔT is temperature difference in °C, q is dissipated power in W, and R is thermal resistance in °C/W.

Thermal Resistance of Solder Attachment

The temperature distribution on the chip of different voiding percentages and different void locations is shown in Figs. 8 and 9. The trend of temperature distribution was almost the same for different voiding percentages and different void locations. The distribution was circular. The outer chip surface has relatively lower temperature. And the left side had a higher temperature compared to the right side.

But the maximum chip temperature of different voiding percentages and void locations was significantly different, as shown in Table 4. With the increase in void sizes, the chip temperature increased. The maximum chip temperature increased 0.8°C compared to no voids when the voiding percentages was 5%. And it increased to 5.1° and 27.2°C when the voiding percentages were 20 and 79%, respectively. The changes in the maximum chip temperature were relatively small (<1°C) for different void locations.

Thermal resistance compared with the case no voids is also listed in Table 4. With increasing void size, the thermal resistance increased. The thermal resistance increased 1.06% compared to no voids when the voiding percentage was 5%, and it increased to 6.53 and 27.18% when the voiding percentages were 20 and 79%, respectively.

For void locations, the closer the voids were to the chip side, the larger the thermal resistance when the voiding percentage was 10%. The thermal resistance increased 1.11% when the voids were at the corner, and it increased to 2.03% when the voids were close to the center of the heat-sink attachment compared with no voids. However, the effect of void location is less significant than voiding percentages.

Experimental Validation

Experimental Procedure

Figure 10A shows the photo of the sample for experimental validation, and Fig. 10B shows the four Dpak devices with higher magnification.

The thermal shock tests were performed in the range –40° to 125°C, with 15 min dwell at –40°C and 75 min dwell at 125°C. Eleven boards were subjected to thermal shock until 3000 cycles. The detailed analysis methods have been introduced in a previous paper (Ref. 13).

Experimental Results

Voiding Percentages

The typical heat-sink attachment of the specimen had big voids from one to three and many small voids. The range of voiding percentages was from 33 to 48%, and the average voiding percentage was 37.5%. An X-ray image of a typical specimen is shown in Fig. 11.

Solder Fatigue and Delamination between Cu/Cu_3Sn

Figure 12 shows SEM images of a cross section after 3000 thermal shock cycles.

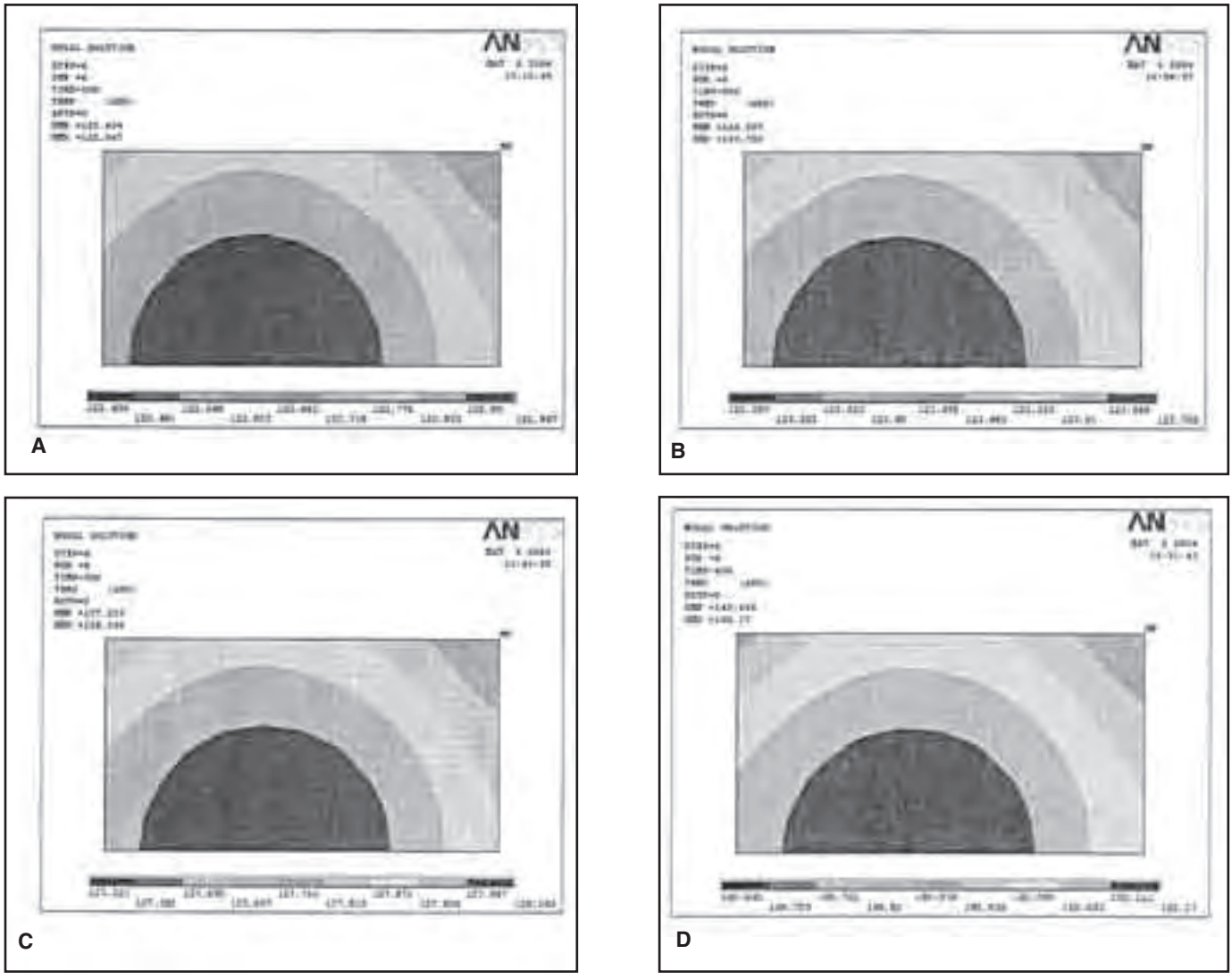


Fig. 8 — The temperature distribution on the chip from topside of different heat-sink attachment voiding percentages. A — 0%; B — 5%; C — 20%; and D — 79%.

Table 4 — Thermal Analysis Result of Simulation

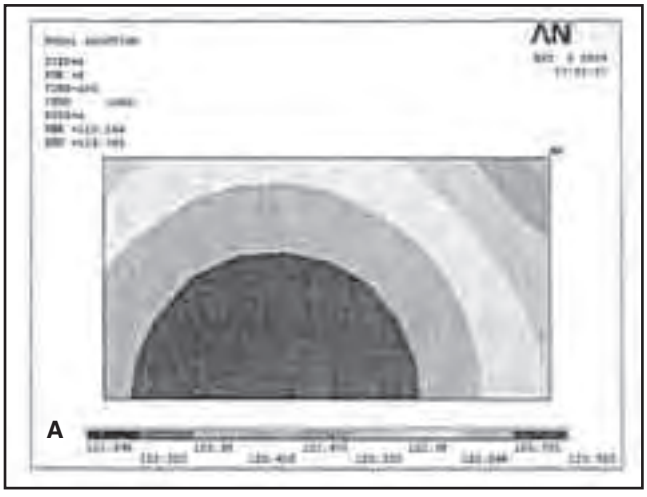
Void percentages (%)	Max chip temp (°C)	ΔT (°C)	Thermal resistance (°C/W)	Increase in thermal resistance as compared to heat-sink attachment with no void (%)
0	122.947	72.947	72.947	0
5	123.726	73.726	73.726	1.06
20	128.045	78.045	78.045	6.53
79	150.170	100.170	100.170	27.18
10–I	123.762	73.762	73.762	1.11
10–II	124.421	74.421	74.421	1.98
10–III	124.456	74.456	74.456	2.03

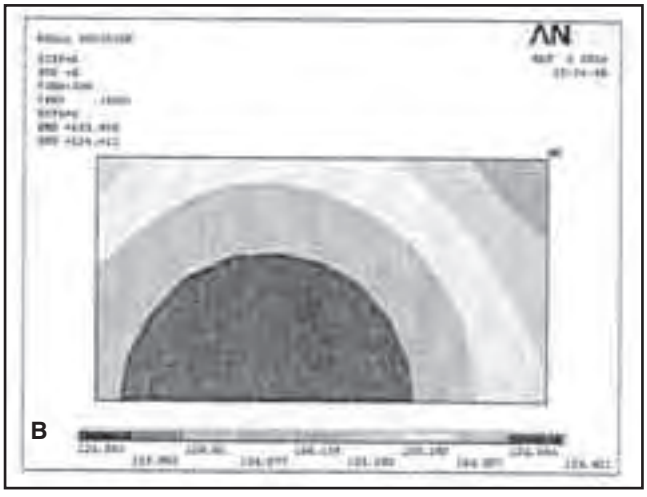
Besides voids, only small solder joint fatigue cracks were found. These fatigue cracks were found either at the two ends of the cross section where the distance to neutral point (DNP) was largest or initiated at a large void location and propagated into the solder. Unexpectedly, the dominant degradation was found to be Kirkendall voids at along almost the whole Cu/Cu_3Sn interface, but not solder fatigue. More detailed experiment results can can be found in a previous paper (Ref. 13).

Discussion

The FEM results showed that the increase in maximum equivalent plastic strain was less than 3.5%, even when the voiding percentage reached 79%. The thermal shock experimental test also confirmed that the heat-sink attachment with large voiding percentages (voiding percentages ranged from 33 to 48%) had a thermal shock cycle lifetime above 3000 cycles, and the dominant degradation mechanism was not solder fatigue but interface delamination due to Kirkendall effects.

The specimens subjected to the present investigation typically contain 1–3 big voids and many small voids. In all cases, experimental validation confirmed that the major failure mode is interfacial degradation due to Kirkendall voids, not solder fatigue. So although several large voids and one large void with equal size may perform differently in thermal-mechanical performances, the present single-void approach is enough to provide an insight to the effects of void percentage and to give rough reference values to their significance. More studies are needed to





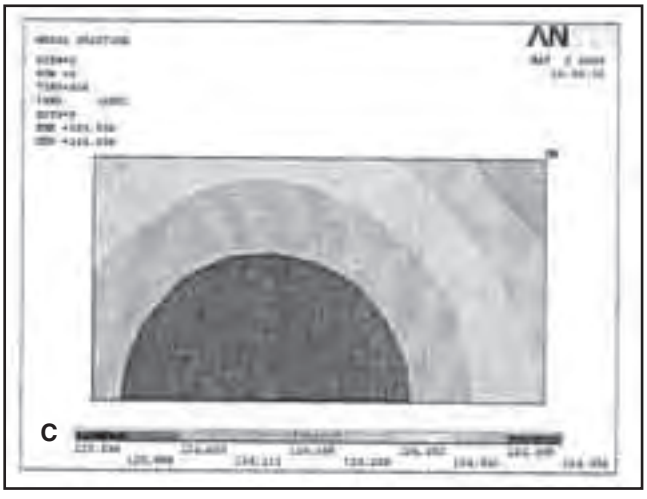


Fig. 9 — The temperature distribution on chip from topside of different heat-sink attachment voids locations. A — 10%-I; B — 10%-II; and C — 10%-III.

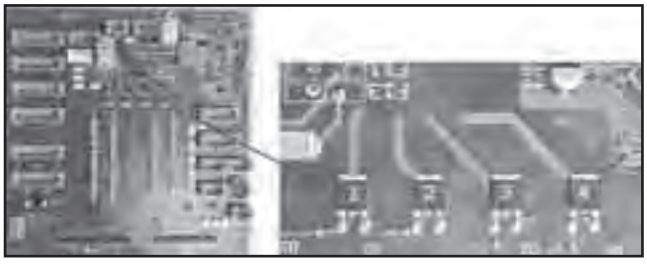


Fig. 10 — A — The surface mount assemblies; B — enlarged Dpak power device on PCB.

get a deeper understanding of multiple large voids. Exact experimental validation of such studies will be impractical, if not possible, as it is very difficult to control the exact void size and location.

Although generally speaking, void size seems to be insignificant to solder attachment lifetime from both FEM and experiment results, some attention needs to be paid to the effect of void locations. When a 10% void exists near the corner of the solder attachment, a location with largest DNP and thus highest stress/strain, the maximum equivalent plastic strain increased by 9.6%.

Different from the effects on thermal-mechanical properties, the voids on heat dissipation show significant effects on voiding percentages, but not too much on void location.

When the void percentage was 5%, the maximum chip temperature increased 0.8°C and thermal resistance increased 1.06% compared to when there were no voids. This was acceptable in general. When the void percentage reached 20%, the maximum chip temperature increased 5.1°C and thermal resistance increased 6.53% compared to when there were no voids. This value may indicate an obvious degraded reliability. The maximum chip temperature increase reached 27.2°C and thermal resistance increased 27.18% compared to when there were no voids when the void percentage further increased to 79%. This is clearly not acceptable from the thermal dissipation point of view.

For void locations, the closer the voids were to the chip side, the larger the thermal resistance when the void percentage was 10%. Because the chip was the only heat source, the further the voids were from the chip, the lower the temperature, and the less effect the voids had on thermal resistance. But the changes in the maximum chip temperature were relatively small (<1°C) for different void locations. The void locations did not have a great effect on the thermal resistance in this case.

The simulation results agree well with common industrial practices. For general heat-sink attachments, the high limit of void percentages is often set to 10%, while for high-performance requirements, 5% is often required. Due to equipment limitation, experimental validation was not performed on heat dissipation.

Conclusions

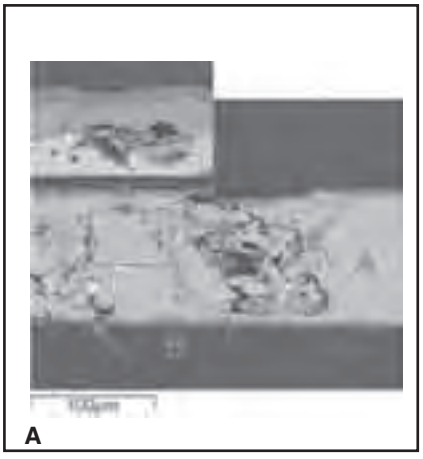
Based on the investigations, the following conclusions can be made.

1. Generally speaking, void percentages did not affect the thermal-mechanical performance of the heat-sink attachment very much.

2. Void location has a much bigger effect on the maximum equivalent plastic strain compared to void percentages. For voids at the relative center of the heat-sink attachment (10%-III), the increase in maximum equivalent plastic strain was 0.434% compared to when there were no voids. For voids at the corner of the heat-sink attachment (10%-I), the increase in maximum equivalent plastic strain reached 9.636%, and the maximum equivalent plastic strain even decreased 0.438% when the voids were at location 10%-II.

3. The void percentages had a significant effect on thermal dissipation. With the increase in void percentages, chip temperature and thermal resistance increased. The thermal resistance increased 1.06% compared to no voids, and it increased to 6.53 and 27.18% when the void percentages were 20 and 79%, respectively. But the effect of void location on thermal dissipation was relatively small, and the changes in the maximum chip temperature were less than 1°C for different void locations.

Fig. 11 — X-ray image of typical specimen in this investigation (voiding percentages, 37.6%).



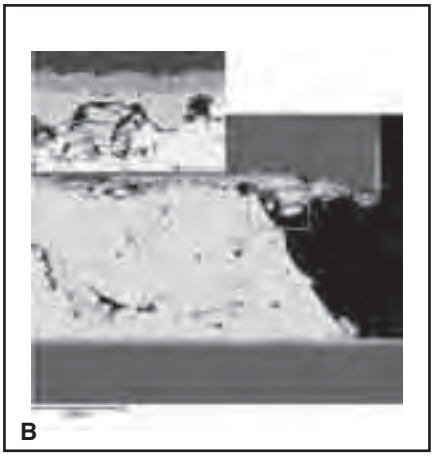


Fig. 12 — Typical SEM images of a cross section after 3000 thermal shock cycles. A — Delamination between Cu/Cu_3Sn; B — solder fatigue.

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Preparation of Manuscripts for Submission to the *Welding Journal* Research Supplement

All authors should address themselves to the following questions when writing papers for submission to the Welding Research Supplement:

- Why was the work done?
- What was done?
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- What is the significance of your results?
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2) **Introduction.** A short statement giving relevant background, purpose, and scope to help orient the reader. Do not duplicate the abstract.

3) **Experimental Procedure, Materials, Equipment.**

4) **Results, Discussion.** The facts or data obtained and their evaluation.

5) **Conclusion.** An evaluation and interpretation of your results. Most often, this is what the readers remember.

6) **Acknowledgment, References and Appendix.**

Keep in mind that proper use of terms, abbreviations, and symbols are important considerations in processing a manuscript for publication. For welding terminology, the *Welding Journal* adheres to AWS A3.0:2001, *Standard Welding Terms and Definitions.*

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