Soldering to Thin Film Hybrid Microcircuits

Candidate solder alloys are evaluated for production use to minimize problems of gold solution, sluggish wetting, brittleness, limited thermal fatigue resistance and limited rework ability

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ABSTRACT. This paper discusses soldering to thin film gold hybrid microcircuits and characterizes the aspects of solderability, such as: (1) extent of gold solution and intermetallic compound layer formation, (2) solder joint shear strength after exposures to operating, burn-in, and rework temperatures and (3) joint shear strength after thermal cycling. The effects on the stability of TA_2N resistors from the soldering flux and various flux cleaning techniques is also presented.

Introduction

Certain appliqué components, cross-overs, lead frames, and mechanical parts can be attached to thin film hybrid microcircuits (HMC's) by welding, thermocompression wire or ribbon bonding, brazing, or soldering.

Soldering is a desirable technique in that it is applicable to batch processing, could permit repair or replacement of defective parts without damaging the thin film network (TFN), and provides better radio-frequency intraconnections when compared with conventional thermocompression wire or ribbon bonding.

The tendency of gold to rapidly dissolve in traditional tin-lead solder alloys can result in such undesirables as sluggish wetting, brittleness, limited thermal fatigue resistance, and limited reworkability. These characteristics prompted efforts to pursue the use of certain lead-indium alloys that are reported as having soldering properties similar to eutectic tin-lead while exhibiting a lower gold absorption rate and improved fatigue life (Ref. 1).

The soldering technology used for Atomic Energy Commission HMC's is further compounded by thermal and mechanical environmental requirements. AEC HMC's, which are designed by Sandia Laboratories, Albuquerque and produced at Bendix, Kansas City, typically: (a) operate in thermal environments approaching 125 C, (b) are burned-in at 150 C for 96 h, (c) experience thermal shocks from -55 C to +150 C, and (d) are exposed to various mechanical environments of vibration, shock and centrifuge after assembly. The melting point (or range) of the solder alloy selected must exceed 150 C and must not exceed 300 C — preferably not exceed 250 C because of possible adverse affects on tantalum nitride thin film resistors. The melting point of the solder must also be such as to allow subsequent solder attachment of the packaged HMC into a printed wiring board assembly.

A study was made to determine and characterize material and processing requirements for producing solder joint intraconnections on 3 micron (118 microin.) and 6 micron (236 microin.) gold metallized thin film HMC's with particular emphasis placed on the 50Pb-50In alloy.

This paper presents selected topics of the study pertinent to solder joint characterization and resistor stability effects from soldering flux and post-solder cleaning processes.

Materials

The metallization system used throughout this study consisted of a resistive layer of sputtered tantalum nitride approximately 0.06 microns (2.4 microin.) thick followed by approximately 0.02 microns (0.8 microin.) of evaporated chromium for adhesion and either 3 or 6 microns

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of an evaporated gold conductive layer. These metallizations were deposited onto alumina substrates in a manner representative of typical production or onto copper substrates where extensive metallographic studies were planned to examine gold solution characteristics. All of the 3 micron gold test specimens were made during one sputtering and evaporation batch and all of the 6 micron gold test specimens were likewise made during one batch to minimize batch to batch processing variations.

Candidate solder alloys of 50Pb-50In, 75Pb-25In, 81Pb-19In, 63Sn-37Pb, 95Sn-5Ag, and a 62Sn-36Pb-2Ag alloy (Sn62 per QQ-S-571) were characterized and evaluated during this study for possible production use.

Activity

Solderability

Solderability determinations were made with a technique similar to the area of spread and spread factor method used by Pessel and others (Refs. 2,3). A controlled volume of solder was melted and allowed to spread upon the test surface for a specific length of time under controlled conditions. The maximum height of the solder was measured and a percent spread factor was calculated from:

$$\text{Spread factor} = (D-H)/D \times 100$$

where D is the diameter of a sphere with a volume equal to the volume of the solder used, and H is the measured height of the solder spread. The better the solderability of a candidate solder alloy, the larger the spread factor. A spread factor greater than 80% is considered good and is acceptable for production. Both metallized ceramic and metallized copper specimens were tested.

The melting point or range of the candidate alloys was determined using differential scanning calorimetry techniques. Two solderability test temperatures were arbitrarily chosen as 25 C and 50 C above the nominal liquidus. Surface temperature of the gold metallized specimens was controlled to within ±2 C during solderability testing. The solderability test time began at the first visible indication of melting in the solder alloy. Test times were controlled and varied from 4 to 64 seconds exposure at test temperatures and were reproducible within ±0.2 seconds. After controlled time-temperature exposures, the test specimens were automatically removed from the temperature source and placed upon an air-cooled, heat-sinking platen.

Gold Solution and Compound Formation

After solderability testing, the gold metallized copper specimens were sectioned and metallographically examined to determine the extent of gold solution by the candidate alloys. Metallographic sections were examined both after polishing and after etching. A two-step etching process was used to enhance metallurgical details. The specimens to be etched were first swab etched with a 1:1 solution of 10% KCN and 3% H_2O_2, rinsed and dried, then followed with a swab etch with Vilella's reagent (2 gm picric acid - 10 ml HCL - 200 ml ethyl alcohol). These metallographic sections were representative of gold solution resulting from controlled time and temperature exposures of 25 C and 50 C above the liquidus temperature of the candidate alloy.

Intermetallic compound formation of the candidate alloys with gold was examined optically and electron-optically with particular emphasis placed on the 50Pb-50In alloy. Scanning electron microscopy (SEM) and electron microprobe (EPA) techniques were used to examine metallographic sections of the 50Pb-50In alloy on gold metallized ceramic and copper samples in the as-cast condition and after various times at temperatures of 125, 135, 150, 160, and 170 C.

Shear Strength Determinations

Shear tests were conducted with as-cast solder joints and solder joints that had been exposed to temperatures of 125 C, 150 C, and 200 C for times up to 128 h. These temperatures were chosen because they are representative of HMC operation, burn-in, and rework conditions. Applique capacitor* solder joints on metallized ceramic test patterns (Fig. 1) were made with candidate solder alloys and destructively tested in shear using a Unitek® Micro-pull tester modified to push the capacitors from the substrate in shear at a rate of 8.9 cm (3.5 in.) per minute. Test specimens were also thermal cycled between -40 and 150 C from 10 to 500 cycles and destructively tested in

**A-case, porcelain chip capacitors provided by American Technical Ceramics, Huntington Station, N.Y.*

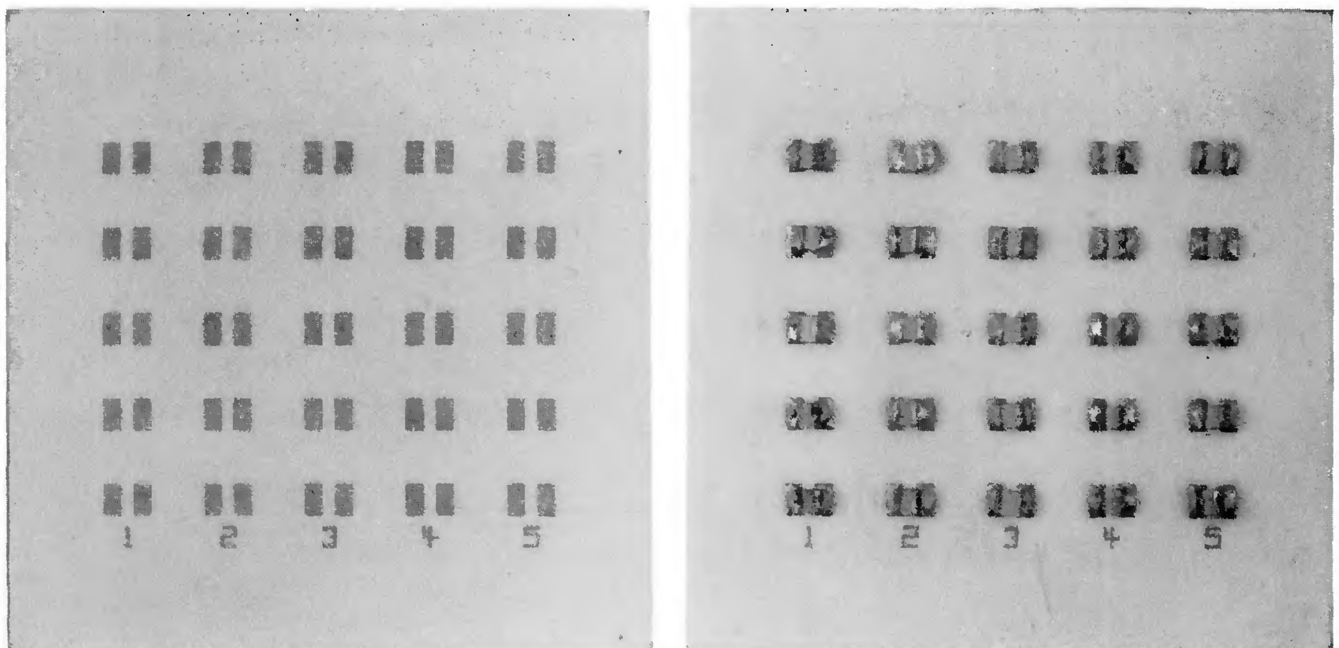


Fig. 1 — Metallized ceramic test pattern and soldered specimen X3.5, reduced 30%

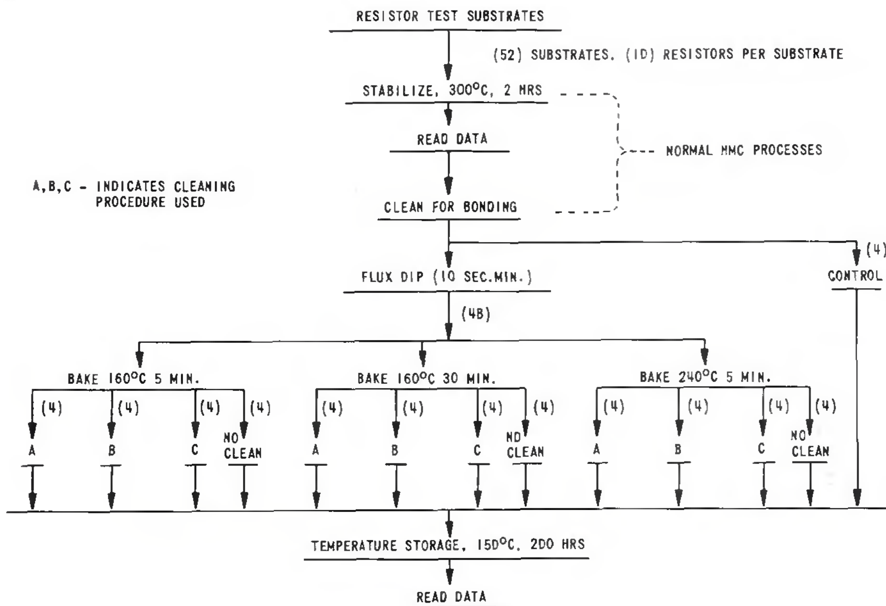


Fig. 2 — Resistor stability testing sequence used to determine the effects of solder flux residue and cleaning procedure upon tantalum nitride thin film resistors

Table 1 — Cleaning Procedures for Flux Removal from HMC Resistor Test Substrates

A. Room temperature trichloroethylene wash. Wash for minimum of 5 min, using soft brush to assist in flux removal.

B. Boil in trichloroethylene for 10 min minimum. Rinse in room temperature isopropyl alcohol for 10 s minimum.
Boil in detergent solution (IGEPAL CO-710 and DI water) for 10 min minimum.
Rinse in room temperature DI water for 10 s minimum.
Rinse in hot flowing DI water for 10 s minimum.
Dry by blow-off with dry nitrogen.

C. Wash in AP20, room temperature, minimum of 3 min. Use soft brush to assist in flux removal.

shear. The 95Sn-5Ag alloy was not studied during this and subsequent investigations because of changed design requirements. After testing, solder joint failure modes were examined with the SEM and an optical microscope.

Determination of Resistor Stability

Resistor stability is determined by calculating the percent change in resistance at room temperature after 200 h exposure at 150 C. Acceptable resistors must not change more than 0.2%. An evaluation was made to determine the effects of solder flux residue on resistor stability. The resistor stability testing sequence is given in Fig. 2 and the three solder flux cleaning procedures evaluated are given in Table 1.

Discussion of Results

Solderability

Reproducible results could not be obtained without the use of a soldering flux. The use of a flux was necessary to obtain the desired solder wetting and flow. Acceptable fluxes for our applications are rosin base fluxes defined by Mil-F-14256, Type RMA.

A summary of the solderability test results is given in Table 2. Review of the data indicates that the solderability (wetting and area of spread) of the lead-indium alloys was more sensitive to time and temperature than were the tin-containing alloys. In

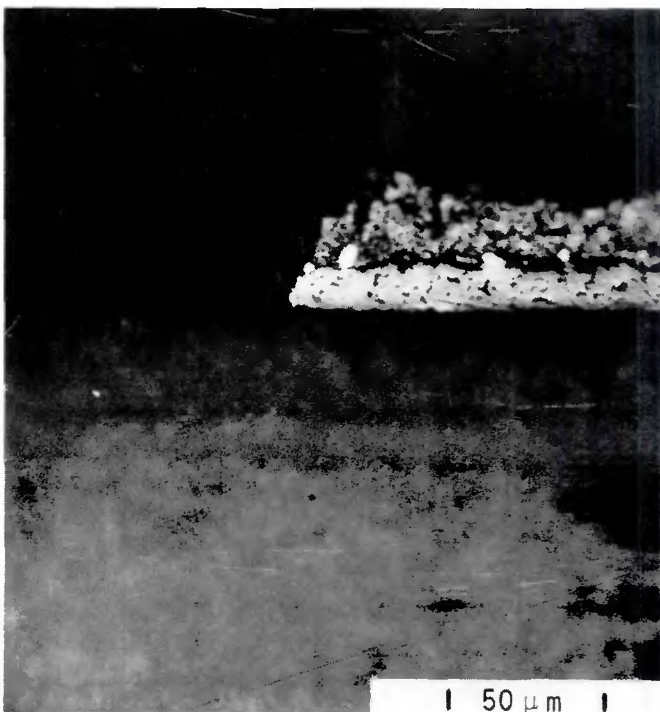


Fig. 3 — Chip capacitor solder joints of 50Pb-50In subject to simulated power burn-in of 96 h at 150 C and shear tested. (Left) the chip failed by compound layer shearing from the tantalum nitride resistive layer

general, the lead-indium alloys must be held longer at temperature to obtain a spread factor similar to those of the tin-containing alloys. When the test temperatures were increased, the trend was still apparent. There was no significant difference in the measured solderability of the ceramic or copper test specimens.

While testing the 81Pb-19In alloy at 50 C above the liquidus, the rosin base solder flux was observed to darken and retard the solder spread. This observation is in keeping with the temperature-sensitivity aspects of rosin-type fluxes discussed by Manko (Ref. 4). The solderability results indicated that, from our assembly soldering standpoint, any of the candidate alloys except 81Pb-19In could be used to obtain satisfactory wetting and flow needed for large solder fillets on applique parts.

Gold Solution and Intermetallic Compound Formation

The purpose of the solution and compound formation investigations was not to characterize the reaction kinetics but rather to determine whether gold metallization remained on the substrate after soldering and after HMC environmental tests. Intermetallic compound formation was investigated after metallographically examining chip capacitor solder joints made with 50Pb-50In solder that had been exposed to a simulated power burn-in of 96 h at 150 C. It was found that all of the gold metallization on the substrate had been converted to an intermetallic compound layer(s) (Fig. 3).

Metallographic examination of the test specimens revealed that four second and longer exposures to typical soldering temperatures was sufficient time for the tin-containing alloys to dissolve and remove all the gold metallization from both the 3 micron and 6 micron specimens. Apparently, the tin-containing alloys first alloyed with the gold on the substrate to form platelets of intermetallic compounds that would separate and disperse themselves within the bulk solder alloy. Toward the edge of the meniscus of the solder spread, however, some gold remained on the substrate and in this region a continuous layer of intermetallic compound was observed on the gold. The gold remaining on the substrate was thickest at the edge of the meniscus of the solder spread and decreased in thickness, until it became nonexistent away from the meniscus toward the center of the solder spread.

It was noted that minimum soldering temperatures and short soldering times (typically one second) could be used with the tin-containing alloys to minimize the extent of gold solution and retain some gold metallization on the conductor path. This approach, however, resulted in continuous layers of gold-tin intermetallic compounds between the solder and the remaining gold across the entire interface under the solder.

Metallographic examination of the indium-containing alloys revealed that, in most cases, a very thin intermetallic compound layer formed on the gold after exposure to typical soldering temperatures and times. As exposure times were increased, the compound layer became thicker and, after a 64 s exposure to typical soldering temperatures, all the gold on the substrate was observed to be converted to a continuous compound layer(s).

The exception was the 81Pb-19In alloy. In this case, short exposure times at soldering temperature allowed all the gold to form a continuous compound layer on the substrate except in the region near the edge of the solder meniscus where the compound separated to become small, discontinuous particles dispersed within the bulk solder with no gold remaining on the substrate.

In order to evaluate the effects of HMC environmental tests on intermetallic compound formation, controlled volumes of 50Pb-50In solder alloy were cast onto gold metallized ceramic test specimens. Casting was done with flux in a manner similar to soldering except time and temperature were minimized.

Table 2 — Solderability Data

Solder	Nominal test temperature	Test time, seconds	Avg. spread factor, % 3 micron gold	Avg. spread factor, % 6 micron gold
1. 50Pb-50In	234 C (453 F)	4	56.11	53.78
		8	60.00	63.19
		16	65.37	77.20
		64	81.71	84.20
	260 C (500 F)	4	63.97	72.77
		8	70.97	72.77
		16	79.77	83.74
		64	80.94	86.38
2. 63Sn-37Pb	209 C (408 F)	4	76.26	74.32
		8	79.38	78.60
		64	89.11	87.94
	233 C (451 F)	4	80.55	78.60
		8	80,93	81.17
		64	90.66	88.33
3. 75Pb-25In	289 C (552 F)	4	66.88	75.07
		8	72.97	77.01
		16	78.34	82.08
		64	77.40	80.91
	312 C (593 F)	4	82.86	83.64
		8	81.30	82.32
		16	84.62	82.47
		64	85.82	85.20
4. 81Pb-19In	305 C (581 F)	4	69.93	64.85
		8	67.58	69.54
		16	73.44	76.02
		64	78.91	78.36
	331 C (628 F)	4	72.66	73.83
		8	75.00	79.30
		16	74.62	80.08
		64	70.71	78.52
5. 95Sn-5Ag	262 C (504 F)	4	66.11	68.84
		8	66.11	68.06
		64	77.41	73.12
	290 C (554 F)	4	70.01	66.11
		8	85.98	91.43
		64	89.87	93.77
6. 62Sn-36Pb-2Ag (Sn62)	214 C (418 F)	4	73.57	72.63
		8	78.10	81.62
		64	87.88	87.88
	240 C (464 F)	4	77.72	80.45
		8	82.01	82.01
		64	91.40	90.62

The test specimens were exposed to temperatures of 125 C, 135 C, 150 C, and 170 C for various times ranging from zero time (representative of as-cast conditions) to 128 h at each temperature. Samples were taken throughout the evaluation, metallographically cross-sectioned and examined. Intermetallic compound layers that formed as a result of the exposure parameters were measured and plotted as total compound layer thickness vs. exposure time at each temperature (Fig 4). The activation energy can be derived from these data by arbitrarily defining a failure time as the time at temperature necessary for the intermetallic compound layer (or total layers) to attain a predetermined thickness and plot failure time against inverse absolute temperature.

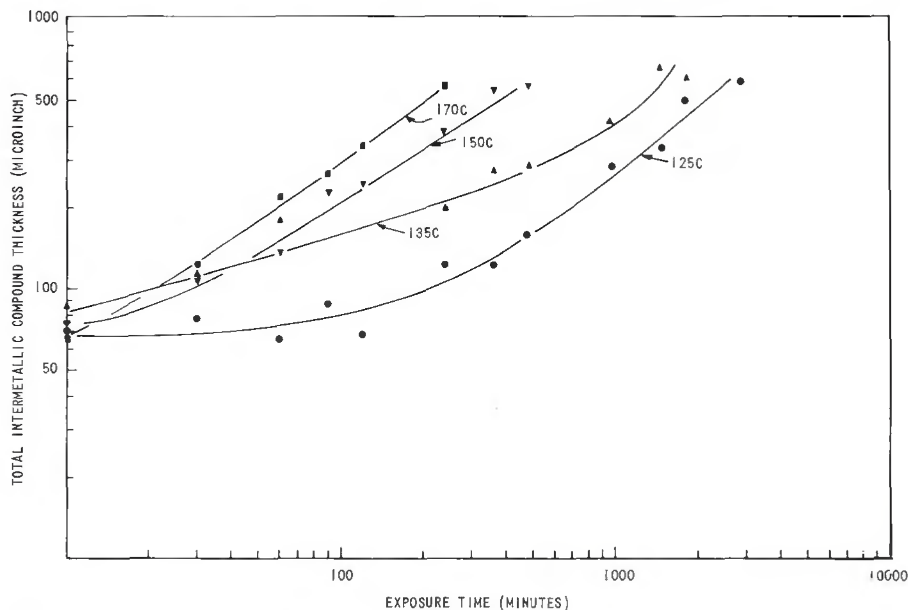


Fig. 4 — Total intermetallic compound layer thickness as a function of exposures at test temperatures

Metallographic examination of the layer growth specimens revealed that the total compound thickness consists of at least two and possibly three separate layers (Fig. 5). To confirm these observations, EPA traces were made across similar specimens. The EPA traces revealed that the total compound layer probably contains separate layers of the compound AuIn and the compound $AuIn_2$. Lead was also detected within the compound layers.

The most significant observation made during this evaluation was the rapid intermetallic compound layer formation at temperatures of 150 C and 125 C which represent HMC power burn-in and operational temperatures. Figure 6 is a photomicrograph typical of an as-cast 50Pb-50In solder joint. After casting, a thin intermetallic compound layer exists along with a relatively thick layer of unalloyed gold. Figure 7 illustrates a 50Pb-50In solder joint after exposure to power burn-in (96 h at 150 C). The intermetallic compound layer(s) was approximately four times as thick as the initial gold deposit. Also, the edge of the solder meniscus had become

Fig. 5 — Condition of 50Pb-50In solder after 24 h exposure to 125 C environment

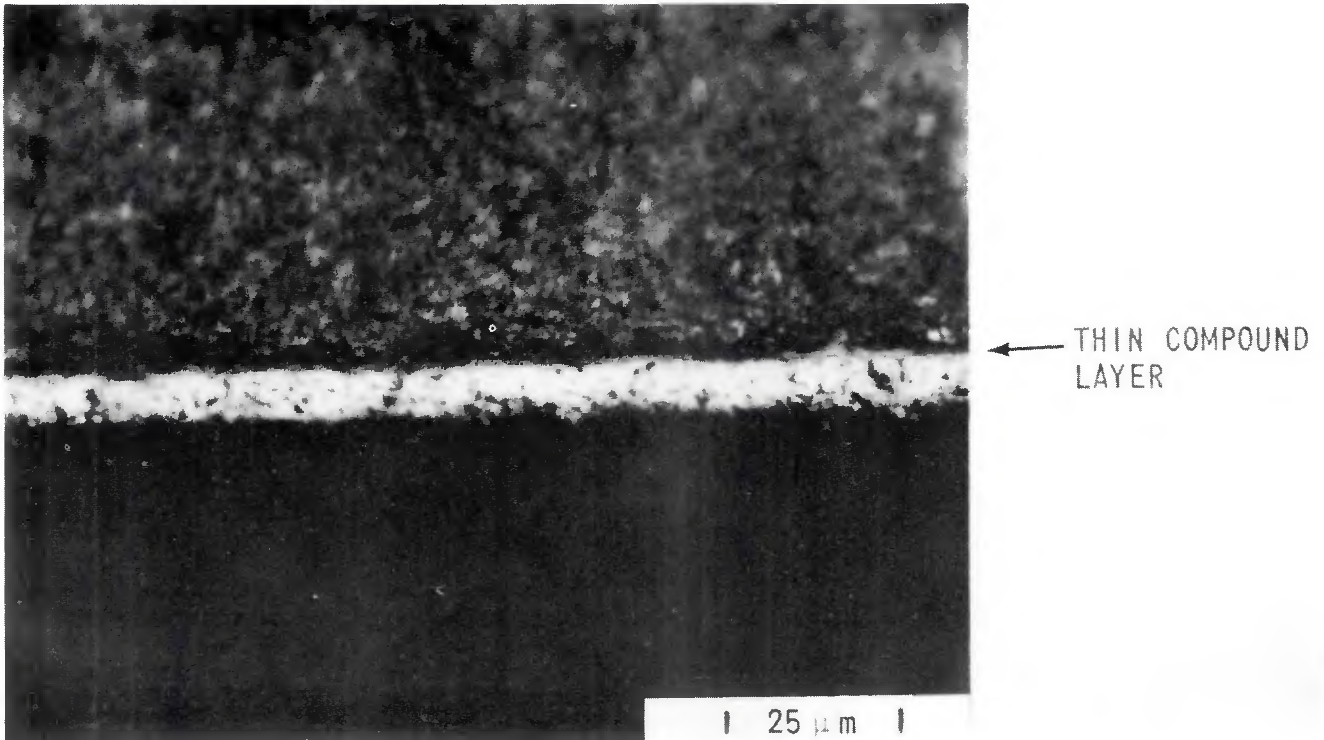


Fig. 6 — As made (as-cast) 50Pb-50In solder joint

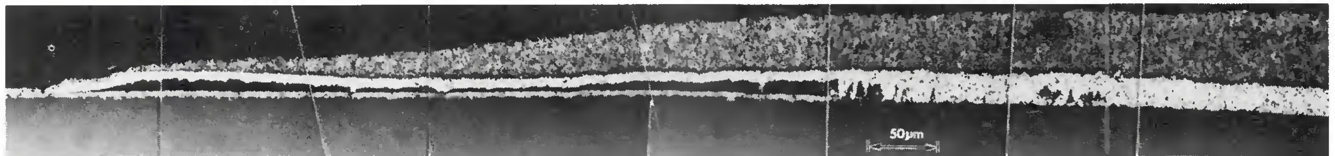


Fig. 7 — Condition of 50Pb-50In solder cast on a 6 m gold metallized specimen after 96 h at 150 C

separated from the resistive layer on the substrate. This separation was probably caused by the growth of the intermetallic compound layer(s).

Shear Strength Properties After Thermal Aging

Applique capacitor solder joints were destructively tested in shear after various thermal exposures to determine if their structural integrity had been significantly degraded as a result of thermal exposures.

All capacitor terminations were pre-tinned with the candidate alloy and each joint was made using a standard size preform of the test alloy in an attempt to make all solder joints uniform in size. An externally applied soldering flux was used during specimen preparation to obtain the desired wetting and flow.

Shear strength data, plotted as a function of time at various temperatures, is shown in Fig. 8. This can be considered representative of the thermal aging effects on the tin-containing and lead-indium solder joint shear strength. Solder joint shear strength appeared to be sensitive to thermal aging in that the initial, as-cast joint strength decreased after

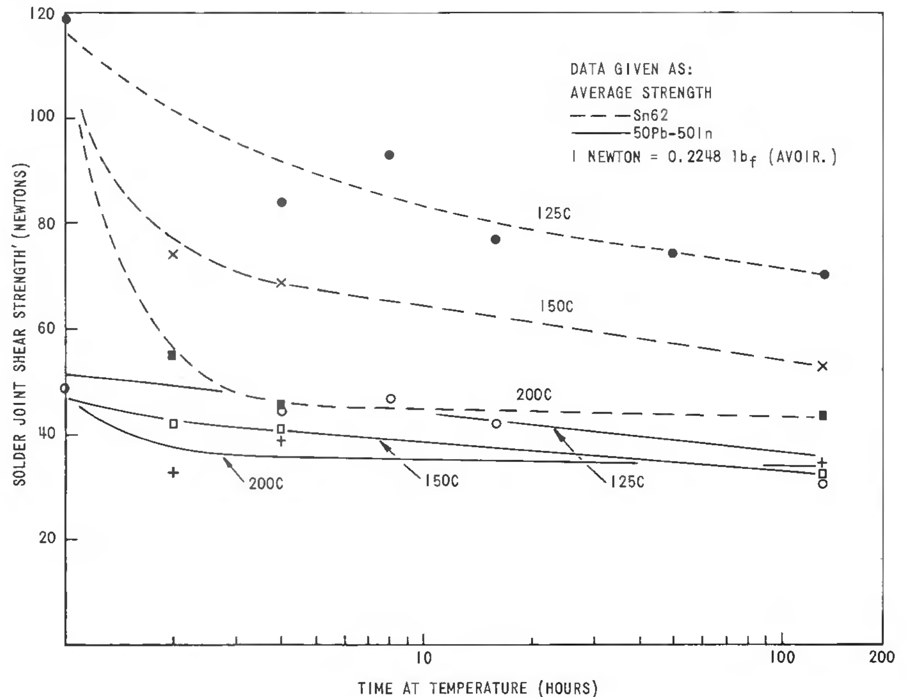


Fig. 8 — Representative thermal aging effects on shear strength of chip capacitor solder joints

thermal exposure. The decrease in shear strength did not appear to be a linear relation; rather, it appeared to be an exponentially decreasing rela-

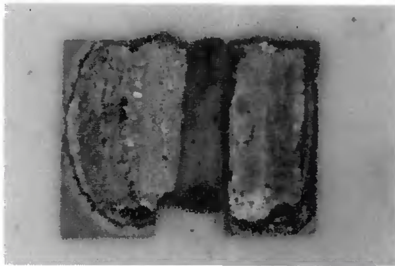
tion. These shear strength data could possibly be related to layer growth in such a manner that what is ultimately being measured is the adhesive strength of the compound layer to the tantalum nitride resistive layer on the substrate after various thermal aging times.

After shear strength testing, failure modes were examined optically and with the SEM. Typical failure modes are illustrated in Fig. 9. Mode 2 is the most desirable failure because it allows subsequent rework of the joint and because it is also indicative of a solder joint which can survive the prescribed thermal and mechanical environments without damage to the HMC metallization or to the chip capacitor.

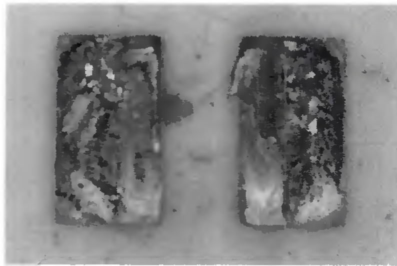
The typical failure mode of the tin-containing alloys (62Sn-36Pb-2Ag, 63Sn-37Pb) can best be described as the entire solder joint fillet — bulk solder alloy and entire intermetallic compound layers — separating from the Ta_2N resistive layer on the ceramic substrate (Mode 3 in Fig. 9). The atypical failure modes of the tin-containing alloys varied considerably and included: (a) ceramic chip failure, (b) chip metallization failure, (c) substrate metallization failure, and (d) failures within the intermetallic compound layer platelets.

The typical failure mode of the lead-indium alloys (50Pb-50In, 75Pb-25In, 81Pb-19In) can best be described as a bulk solder failure (Mode 2 in Fig. 9). The atypical failure modes were generally combinations of solder alloy failure and intermetallic compound separation from the Ta_2N resistive layer.

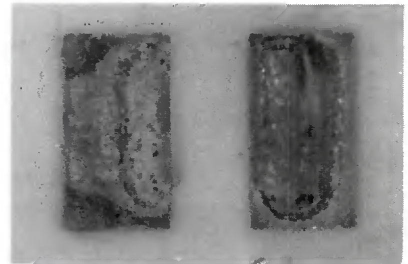
The solder joint shear strengths obtained with lead-indium alloys were, as expected, lower than those of the traditional tin-lead alloys.



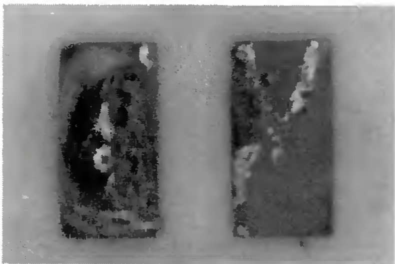
MODE 1 — Capacitor metallization failure either by lack of adhesion to the chip or by dissolving in the solder



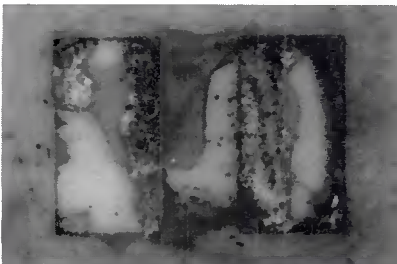
MODE 2 — Solder alloy failure where solder is retained on the capacitor termination and on the substrate metallization



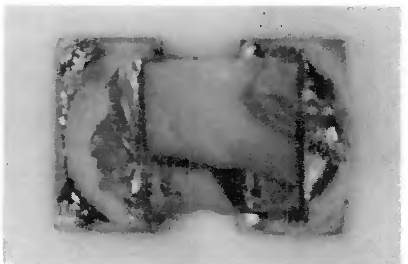
MODE 3 — Separation of the intermetallic compound layer from the resistive layer on the ceramic substrate



MODE 4 — Combination of failure modes 2 and 3

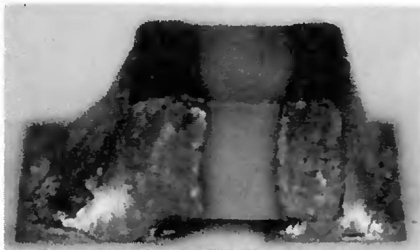


MODE 5 — Separation of resistive layer metallization from ceramic substrate. May be in combination with other failure modes

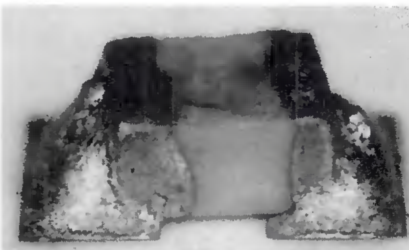


MODE 6 — Ceramic ship capacitor failure

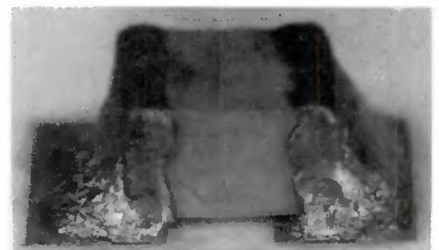
Fig. 9 — Typical failure modes after shear strength testing. X20, reduced 27%



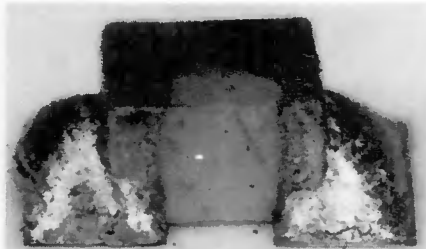
65Sn-36Pb-2Ag



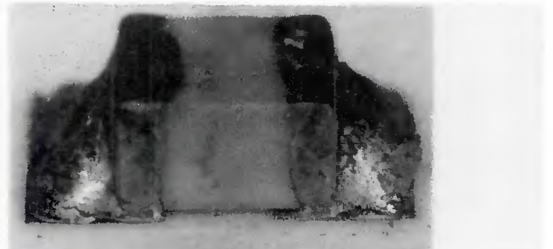
50Pb-50In



63Sn-37Pb



75Pb-25In



81Pb-19In

Fig. 10 — Chip capacitor solder joints after 250 thermal cycles from −40 C 10 min, heat to 150 C in 10 min, hold at 150 C 10 min, cool to −40 C in 2 min. X28, reduced 31%

Table 3 — Thermal Cycling Effects on Chip Capacitor Solder Joints

	Solder joint shear strength — newtons [a]									
	Substrate of 3 micron gold using solders:					Substrate of 6 micron gold using solders:				
Condition	Sn62	50Pb/50In	Sn63	75Pb/25In	81Pb/19In	Sn62	50Pb)50In	Sn63	75Pb/25In	81Pb/19In
As-cast	118.67 (98.3-134.3)	48.48 (40.9-54.7)	69.03 (45.8-86.7)	36.12 (27.6-40.9)	39.41 (33.4-45.4)	81.13 (53.8-10.5)	43.15 (36.9-49.8)	77.04 (34.7-115.7)	35.67 (28.0-42.3)	38.70 (32.0-43.6)
Failure mode	3	2	3	2	2	3	2	3	2	2
10 cycles [b]	99.90 (59.2-150.8)	46.21 (29.4-67.6)	81.09 (67.2-106.8)	40.88 (34.7-50.7)	40.39 (26.7-48.9)	94.70 (72.1-110.8)	42.30 (34.3-56.5)	81.35 (59.2-110.8)	39.54 (25.8-52.9)	50.13 (40.9-66.3)
Failure mode	—	—	—	—	—	—	—	—	—	—
50 cycles [b]	78.42 (68.1-97.0)	43.55 (30.7-57.4)	84.33 (66.7-105.9)	41.81 (27.6-49.4)	44.26 (40.9-48.9)	83.22 (70.7-101.9)	48.97 (41.4-66.3)	83.76 (53.8-105.9)	44.30 (28.5-57.8)	40.83 (26.7-60.5)
Failure mode	3	2	4	2	2	3	4	3	2	4
250 cycles [c]	37.27 (35.6-38.7)	29.45 (24.5-38.7)	46.97 (15.1-65.4)	26.33 (20.0-36.9)	34.34 (13.3-44.9)	43.95 (24.5-72.5)	35.32 (17.8-48.5)	36.74 (22.2-61.8)	31.85 (25.8-45.8)	29.36 (20.5-38.7)
Failure mode	3	2	3,4	2	2	3	2,4	3	2	2,4
500 cycles [c]	25.71 (19.1-35.1)	30.16 (26.7-34.7)	32.65 (23.1-52.6)	20.91 (8.5-28.0)	27.13 (22.2-32.0)	15.75 (.9-24.0)	30.78 (22.2-39.1)	23.04 (7.1-39.6)	19.30 (11.1-27.1)	17.53 (4.5-27.6)
Failure mode	1,3	2	1,3	3	2,3	3,1	2	3	3	3

(a) Data given as AVERAGE and (RANGE). 1 newton = 0.2248 lbf (Avoir.).
(b) -40 C to 125 C
(c) -40 C to 150 C

Shear Strength Properties after Thermal Cycling

The same type of specimens used in the thermal aging evaluation were exposed to various thermal cycling environments, destructively tested in shear after 10, 50, 250, and 500 thermal cycles, after which the failure modes were observed. All candidate alloy solder joints were both visually and mechanically degraded by thermal cycling. Figure 10 contains photomacrographs representative of the visual degradation that occurred during 250 thermal cycles. The degrading mechanism, attributed to thermal stresses resulting from a differential thermal expansion mismatch, generated fatigue cracks in the solder fillet and also initiated separation of the intermetallic compound layers from the Ta_2N resistive metallization. The visible fatigue cracks in the solder and the intermetallic compound separations became more pronounced after 500 cycles.

A summary of the thermal cycling effects on the shear strength of chip capacitor solder joints is given in Table 3. The disparities in the data, revealed by the fact that some joints appeared to initially increase in shear strength, were attributed to variations in the solder joint fillet size where slight variations in the fillet size caused wide variations in the shear strength data. The trend in the data, however, indicated that all candidate alloy solder joints were degraded by thermal cycling.

The reduction in shear strength after thermal cycling was attributed to a reduction in solder joint area resulting from the thermal fatigue cracks in the bulk solder or the separation of the intermetallic compound layer from the substrate metallization, or both.

Table 4 — Results of Test to Determine Effects of Type RMA Flux and Cleaning Procedures upon Tantalum Nitride Thin Film Resistors

		Resistor change, percent		
Bake	Cleaning procedure	Min.	Max.	Avg.
5 MINUTES 160 C	A	.08	.18	.11
	B	.06	.12	.09
	C	.06	.16	.11
	No clean	.07	.20	.16
30 MINUTES 160 C	A	.03	.17	.13
	B	.01	.15	.12
	C	.06	.19	.17
	No clean	.05	.19	.15
5 MINUTES 240 C	A	.06	.14	.13
	B	.00	.12	.08
	C	.03	.20	.15
	No clean	.11	.20	.18
	Control	.00	.14	.07

Resistor Stability

Table 4 summarizes the resistor stability test results. As seen from this table, residual Type RMA flux did not appear to have a significant effect on the stability of Ta_2N resistors. The indication was definite that flux residue did cause a greater average resistance change than shown by the control resistors. Even with no attempt at flux removal, however, the change in resistance did not exceed the maximum allowable 0.2%. A slightly lower average resistance change was evident with the more extensive cleaning procedure (Table 1, B), although the simpler trichloroethylene wash (Table 1, A) would seem satisfactory for most postsolder cleaning applications after HMC solder assembly.

Evaluation of Functional HMC's with Soldered Components

Electrically functional HMC's were solder assembled using the 50Pb-50In solder alloy. Heat sinks; mounting frames; appliqué chip capacitors,

transistors, tuning capacitors, solenoid inductors, transformers; and rf leads were solder attached to various TFN's to make functional HMC's. The functional units were exposed to a burn-in environment of 96 h at 150 C, then subjected to all electrical, thermal and mechanical design requirements and electrically retested. All circuits performed properly after exposure to the prescribed testing environments.

During mechanical testing, the circuits are subjected to a 5000 G's linear acceleration. Linear acceleration done after burn-in is performed in such a manner as to throw the appliqué parts from the HMC. A sample of the devices was overtested in 1000 G acceleration increments until failure. Failures typically occurred between 12,000 G's and 15,000 G's. None of the appliqué component solder joints failed at these G levels. All of the failures were the result of broken ceramic substrates.

Conclusions

1. The solderability of the tin-containing or lead-indium alloys on gold TFN's, measured by their ability to wet and spread when using Type RMA flux, is adequate to assemble hybrid microcircuits.

2. The lead-indium alloys (50Pb-50In, 75Pb-25In) did not dissolve all the gold metallization on the substrate during exposure to typical soldering assembly conditions, while the tin-containing alloys (Sn62, 63Sn-37Pb, 95Sn-5Ag) generally dissolved and removed all the gold metallization on the substrate.

3. After a few hours exposure to HMC operation, burn-in, or repair temperatures, the lead-indium alloys convert all the gold metallization under the solder joint to intermetallic compound layers. During burn-in (exposure of 96 h at 150 C), the growth of intermetallic compound layers can cause a separation of the edge of the solder joint meniscus from the gold metallization.

4. Upon exposure to both thermal and mechanical environments, solder joints made with the candidate alloys were mechanically degraded. The amount of degradation of lead-indium alloys was less than the degradation of tin-containing alloys.

5. Residual solder flux (Mil-F-14256, Type RMA) does not appear to have a significant effect on stabilized tantalum nitride resistors. A simple trichloroethylene wash should be satisfactory for most postsolder cleaning procedures.

6. Either lead-indium or tin-containing alloys can be used to assemble gold thin film HMC's after determining that the assembly solder joints will meet the applicable product requirements. In general, the lead-indium alloys are preferred over tin-containing alloys for solder assembly of gold thin film HMC's because of better joint reworkability. This observation is made because of the slower gold solution rate and the typical failure mode associated with the lead-indium alloys.

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Sandia Laboratories, Albuquerque, defined a tantalum nitride-chromium-gold thin film technology which was transferred to Bendix, Kansas City for production use. Sandia also recommended evaluating 50Pb-50In solder alloys as a method of attaching appliqué components to gold thin films. The work reported herein was derived from Bendix support of the Sandia development, and was done with the support of the U.S. Atomic Energy Commission.

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WRC Bulletin
No. 187
Sept. 1973

"High-Temperature Brazing"

by H. E. Pattee

This paper, prepared for the Interpretive Reports Committee of the Welding Research Council, is a comprehensive state-of-the-art review. Details are presented on protective atmospheres, heating methods and equipment, and brazing procedures and filler metals for the high-temperature brazing of stainless steels, nickel base alloys, superalloys, and reactive and refractory metals. Also included are an extensive list of references and a bibliography.

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WRC Bulletin
No. 197
August 1974

"A Review of Underclad Cracking in Pressure-Vessel Components"

by A. G. Vinckier and A. W. Pense

This report is a summary of data obtained by the PVRC Task Group on Underclad Cracking from the open technical literature and privately sponsored research programs on the topic of underclad cracking, that is, cracking underneath weld cladding in pressure-vessel components. The purpose of the review was to determine what factors contribute to this condition, and to outline means by which it could be either alleviated or eliminated. In the course of the review, a substantial data bank was created on the manufacture, heat treatment, and cladding of heavy-section pressure-vessel steels for nuclear service.

Publication of this report was sponsored by the Pressure-Vessel Research Committee of the Welding Research Council. The price of WRC Bulletin 197 is $5.50. Orders should be sent to the Welding Research Council, 345 E. 47th St., New York, N.Y. 10017.